EE6301 DIGITAL LOGIC CIRCUITS

TWO MARK QUESTIONS WITH ANSWERS

UNIT-I NUMBERING SYSTEMS AND DIGITAL LOGIC FAMILIES

1) What are basic properties of Boolean algebra?

The basic properties of Boolean algebra are commutative property, associative Property and distributive property.

2) State the associative property of boolean algebra.

The associative property of Boolean algebra states that the OR ing of several variables results in the same regardless of the grouping of the variables. The associative property is stated as follows: A+ (B+C) = (A+B) +C

3) State the commutative property of Boolean algebra.

The commutative property states that the order in which the variables are OR ed makes no difference. The commutative property is: A+B=B+A

4) State the distributive property of Boolean algebra.

The distributive property states that AND ing several variables and OR ing the result With a single variable is equivalent to OR ing the single variable with each of the the several Variables and then AND ing the sums. The distributive property is: A+BC= (A+B) (A+C)

5) State the absorption law of Boolean algebra.

The absorption law of Boolean algebra is given by X+XY=X, X(X+Y) =X.

6) State De Morgan's theorem.

De Morgan suggested two theorems that form important part of Boolean algebra. They are,

1) The complement of a product is equal to the sum of the complements. (AB)' = A' + B'

2) The complement of a sum term is equal to the product of the complements. (A + B)' = A'B'

7) Reduce A (A + B)

A (A + B) = AA + AB= A (1 + B) [1 + B = 1]= A.

8) Reduce A'B'C' + A'BC' + A'BC

A'B'C' + A'BC' + A'BC = A'C'(B' + B) + A'B'C

= A'C' + A'BC [A + A' = 1]

= A'(C' + BC)

= A'(C' + B) [A + A'B = A + B]

9) Reduce AB + (AC)' + AB’C (AB + C)

AB + (AC)' + AB’C (AB + C) = AB + (AC)' + AAB'BC + AB'CC

= AB + (AC)' + AB'CC [A.A' = 0]

= AB + (AC)' + AB'C [A.A = 1]

= AB + A' + C' =AB'C [(AB)' = A' + B']

= A' + B + C' + AB'C [A + AB' = A + B]

= A' + B'C + B + C' [A + A'B = A + B]
= A' + B + C' + B'C
=A' + B + C' + B'
=A' + C' + 1
= 1 [A + 1 =1]

10) Simplify the following expression Y = (A + B) (A + C’) (B' + C’)

Y = (A + B) (A + C’) (B' + C’)
= (AA' + AC +A'B +BC) (B' + C') [A.A' = 0]
= (AC + A'B + BC) (B' + C’)
= AB'C + ACC' + A'BB' + A'BC' + BB'C + BCC'
= AB'C + A'BC'

11) Show that (X + Y' + XY) (X + Y') (X'Y) = 0

(X + Y' + XY)(X + Y')(X'Y) = (X + Y' + X) (X + Y’) (X' + Y) [A + A'B = A + B]
= (X + Y’) (X + Y’) (X'Y) [A + A = 1]
= (X + Y’) (X'Y) [A.A = 1]
= X.X' + Y'.X'.Y
= 0 [A.A' = 0]

12) Prove that ABC + ABC' + AB'C + A'BC = AB + AC + BC

ABC + ABC' + AB'C + A'BC=AB(C + C') + AB'C + A'BC
=AB + AB'C + A'BC
=A(B + B'C) + A'BC
=A(B + C) + A'BC
=AB + AC + A'BC
=B(A + C) + AC
=AB + BC + AC
=AB + AC +BC ...Proved

13) Convert the given expression in canonical SOP form Y = AC + AB + BC

Y = AC + AB + BC
=AC (B + B’) + AB (C + C’) + (A + A') BC
=ABC + ABC' + AB'C + AB'C' + ABC + ABC' + ABC
=ABC + ABC' +AB'C + AB'C' [A + A =1]

14) Define duality property.

Duality property states that every algebraic expression deducible from the postulates Of Boolean algebra remains valid if the operators and identity elements are interchanged. If the dual of an algebraic expression is desired, we simply interchange OR and AND operators and replace 1's by 0's and 0's by 1's.

15) Find the complement of the functions F1 = x'yz' + x'y'z and F2 = x (y'z' + yz).
By applying De-Morgan's theorem.

F1' = (x'yz' + x'y'z)' = (x'yz')'(x'y'z)' = (x + y' + z)(x + y +z')
F2' = [x (y'z' + yz)]' = x' + (y'z' + yz)'
= x' + (y'z')'(yz)'

= x' + (y + z) (y' + z')

16) Simplify the following expression

Y = (A + B) (A = C) (B + C)

= (A A + A C + A B + B C) (B + C)

= (A C + A B + B C) (B + C)

= A B C + A C C + A B B + A B C + B B C + B C C = A B C

17) What are the methods adopted to reduce Boolean function?

i) Karnaug map ii) Tabular method or Quine Mc-Cluskey method

iii) Variable entered map technique.

18) State the limitations of karnaugh map.

i) Generally it is limited to six variable map (i.e) more then six variable involving expression are not reduced.

ii) The map method is restricted in its capability since they are useful for simplifying only Boolean expression represented in standard form.

19) What is a karnaugh map?

A karnaugh map or k map is a pictorial form of truth table, in which the map diagram is made up of squares, with each squares representing one minterm of the function.44) Find the minterms of the logical expression

Y = A'B'C' + A'B'C + A'BC + ABC'

Y = A'B'C' + A'B'C + A'BC + ABC'

=m0 + m1 +m3 +m6

=_m (0, 1, 3, 6)

20) Write the maxterms corresponding to the logical expression

Y = (A + B + C’) (A + B' + C') (A' + B' + C)

= (A + B + C’) (A + B' + C') (A' + B' + C)

=M1.M3.M6

= M (1, 3, 6)

PART-B

1. Design a 4-bit binary adder/ subtractor circuit.

a) Basic equations. (4)

b) Comparison of equations. (4)

c) Design using twos complement Circuit diagram. (8)

2. Design a half adder using NAND – NAND logic. (16)

3. Explain how a full adder can be built using two half adders. (16)

4. Design a half adder using at most three NOR gates. (16)

5. Using 8 to 1 multiplexer, realize the Boolean function

T = f(w, x, y, z) = Σ(0,1,2,4,5,7,8,9,12,13) (16)

6. Design a 8421 to gray code converter. (16)

7. Draw the logic diagram of full subtractor and explain its operation. (16)

8. Draw the circuit diagram of NMOS NAND gate and explain its operation. (16)

9. a) Design a full adder circuit using only NOR gates. (4)

b) Draw the circuit of a CMOS two inputs NAND gate (12)

UNIT-II
COMBINATIONAL CIRCUITS

1) What are called don't care conditions?

In some logic circuits certain input conditions never occur, therefore the Corresponding output never appears. In such cases the output level is not defined, it can be either high or low. These output levels are indicated by 'X' or'd' in the truth tables and are called don't care conditions or incompletely specified functions.

2) What is a prime implicant?

A prime implicant is a product term obtained by combining the maximum possible number of adjacent squares in the map.

3) What is an essential implicant?

If a min term is covered by only one prime implicant, the prime implicant is said to be Essential.

4) Define combinational logic.

When logic gates are connected together to produce a specified output for certain specified combinations of input variables, with no storage involved, the resulting circuit is called combinational logic.

5) Write the design procedure for combinational circuits.

- The problem definition
- Determine the number of available input variables & required O/P variables.
- Assigning letter symbols to I/O variables
- Obtain simplified Boolean expression for each O/P.
- Obtain the logic diagram.

6) Define half adder and full adder.

The logic circuit that performs the addition of two bits is a half adder. The circuit that Performs the addition of three bits is a full adder.

7) Define Decoder.

A decoder is a multiple - input multiple output logic circuit that converts coded inputs into coded outputs where the input and output codes are different.

8) What is binary decoder?

A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n out puts lines.

9) Define Encoder.

An encoder has 2n input lines and n output lines. In encoder the output lines generate the binary code corresponding to the input value.

10) What is priority Encoder?

A priority encoder is an encoder circuit that includes the priority function. In priority encoder, if 2 or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.

12) Define multiplexer.

Multiplexer is a digital switch. If allows digital information from several sources to be routed onto a single output line.

13) What do you mean by comparator?

A comparator is a special combinational circuit designed primarily to compare the relative magnitude of two binary numbers.

14) Write down the steps in implementing a Boolean function with levels of NAND Gates.

- Simplify the function and express it in sum of products.
- Draw a NAND gate for each product term of the expression that has at least two Literals.
- The inputs to each NAND gate are the literals of the term.
- This constitutes a group of first level gates.
- Draw a single gate using the AND-invert or the invert- OR graphic symbol in the second level, with inputs coming from outputs of first level gates.
- A term with a single literal requires an inverter in the first level. How ever if the single literal is complemented, it can be connected directly to an input of the second level NAND gate.

15) Give the general procedure for converting a Boolean expression in to multilevel NAND diagram?

- Draw the AND-OR diagram of the Boolean expression.
- Convert all AND gates to NAND gates with AND-invert graphic symbols.
- Convert all OR gates to NAND gates with invert-OR graphic symbols.
- Check all the bubbles in the same diagram. For every bubble that is not compensated by another circle along the same line, insert an inverter or complement the input literal.

PART-B

1) i) Realize a JK flip flop using SR flip flop. (8)

ii) Realize a SR flip flop using NAND gates and explain its operation. (8)

2) Explain various steps in the analysis of synchronous sequential circuits with suitable example.

3) i) Distinguish between a combinational logic circuit and a sequential logic circuit. (4)

ii) Derive the characteristic equation of SR flip flop T1 PG 257. (8)

iii) Using a JK flip flop, explain how a D flip flop can be obtained. (4)

4) Design a four state down counter using T flip flop. (16)

5) Design a 4-bit synchronous 8421 decade counter with ripple carry. (16)

6) Design a synchronous 3-bit gray code up counter with the help of excitation table. (16)

7) Describe the input and output action of JK master/slave flip flops. (16)

8) Design a MOD-10 synchronous counter using JK flip flops. (16)
9) Realize SR neither flip flop using NOR gates and explain its operation. (16)

UNIT-III
SYNCHRONOUS SEQUENTIAL CIRCUITS

1. What are the classifications of sequential circuits?

The sequential circuits are classified on the basis of timing of their signals into two types. They are,

1) Synchronous sequential circuit. 2) Asynchronous sequential circuit.

2. Define Flip flop.

The basic unit for storage is flip flop. A flip-flop maintains its output state either at 1 or 0 until directed by an input signal to change its state.

3. What are the different types of flip-flop?

There are various types of flip flops. Some of them are mentioned below they are,

(1) RS flip-flop (2) SR flip-flop (3) D flip-flop
(4) JK flip-flop (5) T flip-flop

4. What is the operation of RS flip-flop?

- When R input is low and S input is high the Q output of flip-flop is set.
- When R input is high and S input is low the Q output of flip-flop is reset.
- When both the inputs R and S are low the output does not change
- When both the inputs R and S are high the output is unpredictable.

5. What is the operation of SR flip-flop?

- When R input is low and S input is high the Q output of flip-flop is set.
- When R input is high and S input is low the Q output of flip-flop is reset.
- When both the inputs R and S are low the output does not change.
- When both the inputs R and S are high the output is unpredictable.

6. What is the operation of D flip-flop?

In D flip-flop during the occurrence of clock pulse if D=1, the output Q is set and if D=0, the output is reset.

7. What is the operation of JK flip-flop?

- When K input is low and J input is high the Q output of flip-flop is set.
- When K input is high and J input is low the Q output of flip-flop is reset.
- When both the inputs K and J are low the output does not change
- When both the inputs K and J are high it is possible to set or reset the Flip-flop (ie) the output toggle on the next positive clock edge.

8. What is the operation of T flip-flop?

T flip-flop is also known as Toggle flip-flop.

- When T=0 there is no change in the output.
- When T=1 the output switch to the complement state (ie) the output toggles.

9. Define race around condition.

In JK flip-flop output is fed back to the input. Therefore change in the output results change in the input. Due to this in the positive half of the clock pulse if both J and K are high then output toggles continuously. This condition is called race around condition'.

10. What is edge-triggered flip-flop?

The problem of race around condition can solved by edge triggering flip flop. The term edge triggering means that the flip-flop changes state either at the positive edge or negative edge of the clock pulse and it is sensitive to its inputs only at this transition of the clock.

11. What is a master-slave flip-flop?

A master-slave flip-flop consists of two flip-flops where one circuit serves as a master and the other as a slave.

12. Explain the flip-flop excitation tables for RS FF.

In RS flip-flop there are four possible transitions from the present state to the next state. They are,

- _ 0_0 transition: This can happen either when R=S=0 or when R=1 and S=0.
- _ 0_1 transition: This can happen only when S=1 and R=0.
- _ 1_0 transition: This can happen only when S=0 and R=1.
- _ 1_1 transition: This can happen either when S=1 and R=0 or S=0 and R=0.

13. Explain the flip-flop excitation tables for JK flip-flop

In JK flip-flop also there are four possible transitions from present state to next state.They are,

- _ 0_0 transition: This can happen when J=0 and K=1 or K=0.
- _ 0_1 transition: This can happen either when J=1 and K=0 or when J=K=1.
- _ 1_0 transition: This can happen either when J=0 and K=1 or when J=K=1.
- _ 1_1 transition: This can happen when K=0 and J=0 or J=1.

14. Explain the flip-flop excitation tables for D flip-flop

In D flip-flop the next state is always equal to the D input and it is independent of the present state. Therefore D must be 0 if Qn+1 has to 0, and if Qn+1 has to be 1 regardless the value of Qn.

15. Explain the flip-flop excitation tables for T flip-flop

When input T=1 the state of the flip-flop is complemented; when T=0, the state of the Flip-flop remains unchanged. Therefore, for 0_0 and 1_1 transitions T must be 0 and for 0_1 and 1_0 transitions must be 1.

16. Define sequential circuit.

In sequential circuits the output variables dependent not only on the present input variables but they also depend up on the past history of these input variables.

17. Give the comparison between combinational circuits and sequential circuits.

Combinational circuits Sequential circuits Memory unit is not required Memory unity is Required Parallel adder is a combinational circuit Serial adder is a sequential circuit.

18. What do you mean by present state?

The information stored in the memory elements at any given time define.s the present state of the sequential circuit.

19. What do you mean by next state?

The present state and the external inputs determine the outputs and the next state of the sequential circuit.

20. State the types of sequential circuits?

1. Synchronous sequential circuits 2. Asynchronous sequential circuits

21. Define synchronous sequential circuit

In synchronous sequential circuits, signals can affect the memory elements only at discrete instant of time.

22. Define Asynchronous sequential circuit?

In asynchronous sequential circuits change in input signals can affect memory element at any instant of time.

23. Give the comparison between synchronous & Asynchronous sequential circuits?

Synchronous sequential circuits Asynchronous sequential circuits. Memory elements are locked flip-flops Memory elements are either unlocked flip - flops or time delay elements.

24. What is race around condition?

In the JK latch, the output is feedback to the input, and therefore changes in the output results change in the input. Due to this in the positive half of the clock pulse if J and K are both high then output toggles continuously. This condition is known as race around condition.

25. Give the comparison between synchronous & Asynchronous counters.

Asynchronous counters

- In this type of counter flip-flops are Connected in such a way that output of 1st Flip-flop drives the clock for the next Flipflop
- All the flip-flops are not clocked Simultaneously

Synchronous counters

- In this type there is no connection between output of first flip-flop and clock input of

the next flip – flop

- All the flip-flops are clocked simultaneously

PART B

1. Explain with neat diagram the different hazards and the way to eliminate them. (16)
2. State with a neat example the method for the minimization of primitive flow table. (16)
3. a) Explain in detail about Races. (6)
b) Explain the different methods of state assignment . (10)
4. a) Explain the fundamental mode asynchronous sequential circuit. (8)
b) Briefly explain the pulse mode asynchronous sequential circuit. (8)
5.What are the steps in the analysis and design of asynchronous sequential circuits? Explain with an example. (16)

UNIT-IV
ASYNCHRONOUS SEQUENTIAL CIRCUITS AND PROGRAMMABLE LOGIC DEVICES

1. Explain ROM.

A read only memory (ROM) is a device that includes both the decoder and the OR gates within a single IC package. It consists of n input lines and m output lines. Each bit Combination of the input variables is called an address. Each bit combination that comes out of the output lines is called a word. The number of distinct addresses possible with n input variables is 2n.

2. What are the types of ROM?

1. PROM 2. EPROM 3. EEPROM

3. Explain PROM.

PROM (Programmable Read Only Memory) it allows user to store data or program. PROMs use the fuses with materiallike nichrome and polycrystalline. The user can blow these fuses by passing around 20 to 50 mA of current for the period 5 to 20μs.The blowing of fuses is called programming of ROM. The PROMs are one time programmable. Once programmed, the information is stored permanent.

4. Explain EPROM.

EPROM (Erasable Programmable Read Only Memory) EPROM use MOS circuitry. They store 1's and 0's as a packet of charge in a buried layer of the IC chip. We can erase the stored data in the EPROMs by exposing the chip to ultraviolet light via its quartz window for 15 to 20 minutes. It is not possible to erase selective information. The chip can be reprogrammed.

5. Explain EEPROM.

EEPROM (Electrically Erasable Programmable Read Only Memory). EEPROM also use MOS circuitry. Data is stored as charge or no charge on an insulated layer or an insulated floating gate in the device. EEPROM allows selective erasing at the register level rather than erasing all the information since the information can be changed by using electrical signals.

6**. Define address and word:**

In a ROM, each bit combination of the input variable is called on address. Each bit combination that comes out of the output lines is called a word.

7. What are the types of ROM.?

1. Masked ROM. 2. Programmable Read only Memory

3. Erasable Programmable Read only memory.
4. Electrically Erasable Programmable Read only Memory.

8. What is programmable logic array? How it differs from ROM?

In some cases the number of don't care conditions is excessive, it is more economical to use a second type of LSI component called a PLA. A PLA is similar to a ROM in concept; however it does not provide full decoding of the variables and does not generates all the min terms as in the ROM.

9. What is mask - programmable?

With a mask programmable PLA, the user must submit a PLA program table to the manufacturer.

10. What is field programmable logic array?

The second type of PLA is called a field programmable logic array. The user by means of certain recommended procedures can program the EPLA.

11. List the major differences between PLA and PAL

PLA: Both AND and OR arrays are programmable and Complex Costlier than PAL
PAL:AND arrays are programmable OR arrays are fixed Cheaper and Simpler

12. Define PLD.

Programmable Logic Devices consist of a large array of AND gates and OR gates that Can be programmed to achieve specific logic functions.

13. Give the classification of PLDs.

PLDs are classified as PROM (Programmable Read Only Memory), Programmable Logic Array (PLA), Programmable Array Logic (PAL), and Generic Array Logic (GAL)

14. Define PROM.

PROM is Programmable Read Only Memory. It consists of a set of fixed AND gates Connected to a decoder and a programmable OR array.

15. Define PLA.

PLA is Programmable Logic Array (PLA). The PLA is a PLD that consists of a Programmable AND array and a programmable OR array.

16. Define PAL.

PAL is Programmable Array Logic. PAL consists of a programmable AND array and a fixed OR array with output logic.

17. Why was PAL developed?

It is a PLD that was developed to overcome certain disadvantages of PLA, such as longer delays due to additional fusible links that result from using two programmable arrays and more circuit complexity.

18. Define GAL.

GAL is Generic Array Logic. GAL consists of a programmable AND array and a fixed OR array with output logic.

19. Why the input variables to a PAL are buffered

The input variables to a PAL are buffered to prevent loading by the large number of AND gate inputs to which available or its complement can be connected.

20. What does PAL 10L8 specify?

PAL - Programmable Logic Array

10 - Ten inputs

L - Active LOW Ouput

8 - Eight Outputs

21. What is CPLD?

CPLDs are Complex Programmable Logic Devices. They are larger versions of PLDs with a centralized internal interconnect matrix used to connect the device macro cells together.

22. Define bit, byte and word.

The smallest unit of binary data is bit. Data are handled in a 8 bit unit called byte. A complete unit of information is called a word which consists of one or more bytes.

23. How many words can a 16x8 memory can store?

A 16x8 memory can store 16,384 words of eight bits each

24. Define address of a memory.

The location of a unit of data in a memory is called address.

25. What is Read and Write operation?

The Write operation stores data into a specified address into the memory and the Read operation takes data out of a specified address in the memory.

26. Why RAMs are called as Volatile?

RAMs are called as Volatile memories because RAMs lose stored data when the power is turned OFF.

27. Define ROM.

ROM is a type of memory in which data are stored permanently or semi permanently. Data can be read from a ROM, but there is no write operation.

28. Define RAM.

RAM is Random Access Memory. It is a random access read/write memory. The data can be read or written into from any selected address in any sequence.

29. Define Static RAM and dynamic RAM.

Static RAM use flip flops as storage elements and therefore store data indefinitely as long as dc power is applied. Dynamic RAMs use capacitors as storage elements and cannot retain data very long without capacitors being recharged by a process called refreshing.

30. List the two types of SRAM.

Asynchronous SRAMs and Synhronous Burst SRAMs

31. List the basic types of DRAMs.

Fast Page Mode DRAM,Extended Data Out DRAM(EDO DRAM),Burst EDO DRAM and Synchronous DRAM.

32. Define a bus.

A bus is a set of conductive paths that serve to interconnect two or more functional components of a system or several diverse systems.

33. Define Cache memory.

It is a relatively small, high-speed memory that can store the most recently used instructions or data from larger but slower main memory.

34. What is the technique adopted by DRAMs.

DRAMs use a technique called address multiplexing to reduce the number of address lines.

35.Give the feature of UV EPROM.

UV EPROM is electrically programmable by the user, but the store data must be erased by exposure to ultra violet light over a period of several minutes.

36. Give the feature of flash memory.

The ideal memory has high storage capacity, non-volatility; in-system read and write capability, comparatively fast operation. The traditional memory technologies such as ROM, PROM, EEPROM individually exhibits one of these characteristics, but no single technology has all of them except the flash memory.

37. What are Flash memories?

They are high density read/write memories that are non-volatile, which means data can be stored indefinitely with out power.

38. List the three major operations in a flash memory.

Programming, Read and Erase operation

39. What is a FIFO memory?

The term FIFO refers to the basic operation of this type of memory in which the first data bit written into the memory is to first to be read out.

40. List basic types of programmable logic devices.

1. Read only memory 2. Programmable logic Array 3. Programmable Array Logic

PART B

1. a) Explain the operation of bipolar Ram cell with suitable diagram.
   b) Explain the different types of ROM.
2. What is Ram? Explain the different types of RAM in detail.

3. Draw the circuit of a NMOS two input NOR gate and explain its operation.
4. Discuss about the TTL parameters. Draw the TTL inverter circuit.
5. a) Draw the circuit of TTL NAND gate and explain its operation.
   b) Draw the circuit of NMOS NAND gate and explain its operation.
6. Draw the ECL circuit and explain its operation clearly.
7. Explain the totem circuit of TTL logic family.

UNIT-V
VHDL

1. What is Verilog?

Verilog is a general purpose hardware descriptor language. It is similar in syntax to the C programming language. It can be used to model a digital system at many levels of abstraction anging from the algorithmic level to the switch level.

2. What are the various modeling used in Verilog?

1. Gate-level modeling 2. Data-flow modeling
3. Switch-level modeling 4. Behavioral modeling

3. What is the structural gate-level modeling?

Structural modeling describes a digital logic networks in terms of the components that wake up the system. Gate-level modeling is based on using primitive logic gates and specifying how they are wired together.

4. What is Switch-level modeling?

Verilog allows switch-level modeling that is based on the behavior of MOSFETs. Digital circuits at the MOS-transistor level are described using the MOSFET switches.

5. What are identifiers?

Identifiers are names of modules, variables and other objects that we can reference in the design. Identifiers consists of upper and lower case letters, digits 0 through 9, the underscore character(_) and the dollar sign($). It must be a single group of characters. Examples: A014, a, b, in_o, s_out

6. What are the value sets in Verilog?

Verilog supports four levels for the values needed to describe hardware referred to as value sets.

Value levels Condition in hardware circuits

- 0 Logic zero, false condition
- 1 Logic one, true condition
- X Unknown logic value
- Z High impedance, floating state

7. What are the types of gate arrays in ASIC?

1) Channeled gate arrays 2) Channel less gate arrays 3) Structured gate arrays

8. Give the classifications of timing control

Methods of timing control:

1. Delay-based timing control
2. Event-based timing control
3. Level-sensitive timing control

Types of delay-based timing control:

1. Regular delay control
2. Intra-assignment delay control
3. Zero delay control

Types of event-based timing control:

1. Regular event control
2. Named event control
3. Event OR control
4. Level-sensitive timing control

9 .Give the different arithmetic operators?

Operator symbol Operation performed Number of operands

* Multiply Two
/ Divide Two
+ Add Two
- Subtract Two
% Modulus Two
** Power (exponent) Two

10. Give the different bitwise operators.

Operator symbol Operation performed Number of operands

~ Bitwise negation One
& Bitwise and Two
| Bitwise or Two
^ Bitwise xor Two
^~ or ~^ Bitwise xnor Two
~& Bitwise nand Two
~| Bitwise nor Two

11. What are gate primitives?

Verilog supports basic logic gates as predefined primitives. Primitive logic function keyword provides the basics for structural modeling at gate level. These primitives are instantiated like modules except that they are predefined in verilog and do not need a module definition. The important operations are and, nand, or, xor, xnor, and buf(non-inverting drive buffer).

12. Give the two blocks in behavioral modeling.

1. An initial block executes once in the simulation and is used to set up initial conditions and step-by-step data flow.
2. An always block executes in a loop and repeats during the simulation.

13. What are the types of conditional statements?

1. No else statement

    Syntax: if ([expression]) true – statement;

2. One else statement

    Syntax: if ([expression]) true – statement;
    else false-statement;

3. Nested if-else-if

    Syntax : if ([expression1]) true statement 1;
    else if ([expression2]) true-statement 2;
    else if ([expression3]) true-statement 3;
    else default-statement;

PART B

1. Explain the various modeling methods used in VHDL with an example. (16)
2. Explain in detail about the principal of operation of VHDL Simulator. (16)
3. Write the VHDL program for 4 bit counter. (16)
4. Write the VHDL program for full adder in all three types of modeling? (16)
5. Write VHDL program for 4:1 MUX using behavioral modeling. (16)
6. Write VHDL program for encoder and decoder using structural modeling. (16)
7. With an example explain in detail the test bench creation. (16)
8. Write a verilog program for

1) Full Adder. (8)

2) Shift Register. (8)